## AMENDMENTS TO THE CLAIMS

Claims 1-15 (Withdrawn)

16. (Original) An integrated circuit (IC) chip comprising an IC formed on a substrate, the IC comprising:

a first interconnect layer;

a first embedded test circuit comprising a first ring oscillator coupled to a first test load, the first test load comprising an interconnect structure formed in the first interconnect layer; and

a second embedded test circuit comprising a second ring oscillator, the second ring oscillator comprising an unloaded ring oscillator, and the second ring oscillator being substantially similar to the first ring oscillator.

- 17. (Original) The IC chip of Claim 16, further comprising:
  - a second interconnect layer; and
- a third embedded test circuit comprising a third ring oscillator coupled to a third test load, the third test load comprising an interconnect structure formed in the second interconnect layer, and the third ring oscillator being substantially similar to the first ring oscillator.
- 18. (Original) The IC chip of Claim 16, further comprising a third embedded test circuit, the third embedded test circuit comprising a third ring oscillator, wherein the first ring oscillator comprises a first transistor type, and wherein the third ring oscillator comprises a second transistor type.
- 19. (Original) The IC chip of Claim 16, wherein the substrate comprises a wafer, and wherein a plurality of additional ICs is formed on the wafer.
- 20. (Original) The IC chip of Claim 16, wherein the IC comprises a field programmable gate array (FPGA), and wherein the FPGA is configured as a measurement circuit for reading a first output signal from the first embedded test circuit

X-1447 US PATENT 10/742,300 Conf. No.: 5676

circuit and a second output signal from the second embedded test circuit.

Claims 21-22.

(Withdrawn)